the invention to which the claims are directed.

Claims 22-39 are pending in this application. Claims 27-39 have been withdrawn from consideration. Claims 22, 24, and 26 were rejected under 35 U.S.C. §102(b) as clearly anticipated by Hagino, U.S. patent 5,304,821. Claim 23 was rejected under 35 U.S.C. §103(a) as unpatentable over Hagino in view of Clark et al, U.S. patent 5,178,370. Claim 25 was rejected under 35 U.S.C. §103(a) as unpatentable over Hagino.

Addressing now the outstanding rejection to Claims 22, 24, and 26 under 35 U.S.C. §102(b) as anticipated by Hagino, the rejection of Claim 23 further in view of Clark et al, and the rejection of Claim 24 as unpatentable over Hagino, those rejections are traversed by the present response.

It is initially noted that Claim 22 has been amended by the present response to clarify a structure in the present invention. More specifically, Claim 22 has been amended by present response to now further recite that "said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer". According to such a feature in the present invention, and with reference to Figure 3 of the present specification as one example, the third semiconductor layer 43 is interposed between the second semiconductor layer 42 and the bottom of the fourth semiconductor layer 44. Such a feature in the present invention patentably distinguishes Claim 22 from Figure 5 of Hagino.

More particularly, it is clear from Figure 5 of Hagino that the noted third semiconductor layer 12 is not interposed between the noted second semiconductor layer 3 and the noted fourth semiconductor layer 4. Thus, clearly Claim 22, and the claims dependent therefrom, patentably defines over the teachings in Hagino.

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In such ways, the present invention as recited in independent Claim 22, and the claims dependent therefrom, patentably defines over the teachings in Hagino.

Moreover, no teachings in Clark et al can overcome the deficiencies in Hagino.

In such ways, the present invention as recited in independent Claim 22, and the claims dependent therefrom, patentably defines over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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Serial No:
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Amendment Filed on:
July 24, 2001

IN THE TITLE

Please amend the title as follows:

[INSULATED GATE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF]

INSULATED GATE SEMICONDUCTOR DEVICE WITH LOW ON VOLTAGE AND MANUFACTURING METHOD THEREOF

IN THE CLAIMS

Please amend Claim 22 as follows:

--22. (Amended) An insulated gate semiconductor device, comprising:

a first semiconductor layer of a first conductivity type having first and second main surfaces on opposite sides thereof;

a second semiconductor layer of a second conductivity type provided on said first main surface of said first semiconductor layer;

a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer, wherein said third semiconductor layer is interposed between

said second semiconductor layer and a bottom of said fourth semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on a portion of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said portion through said insulating film so that said portion forms a channel region.--